The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* MARK FLOOD, MARK RUETTY, and ANTHONY CACHAT.

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Appeal No. 2006-3148
Application No. 09/862,941
Technology Center 2100

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Decided: February 9, 2007

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Before JAMES D. THOMAS, JOSEPH F. RUGGIERO, and ALLEN R. MACDONALD, *Administrative Patent Judges*.

MACDONALD, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-52.

## THE INVENTION

The disclosed invention relates to the art of industrial controls and more particularly pertains to an apparatus for multi-chassis configurable time synchronization (Specification 1).

Representative claim 1 is illustrative:

1. A time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising;

a processor interface for interfacing the synchronization apparatus with a host processor;

a transmitter adapted to transmit synchronization information and data to a network in the control system;

a receiver adapted to receive synchronization information and data from the network; and

a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor.

## THE REFERENCES

The Examiner relies upon the following references as evidence of anticipation and unpatentability:

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| Voth | US 6,199,169 B1 | Mar. 6, 2001 |
| Rasmussen | US 6,449,732 B1 | Sep. 10, 2002 |
| Kuribayashi | US 6,775,246 B1 | Aug. 10, 2004 |

## THE REJECTIONS

The following rejections are on appeal before us:

1. Claims 1-7, 13-28, 30-34, 38-46, and 48-52 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Voth.
2. Claims 8-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Voth in view of Rasmussen.
3. Claims 29, 35, 36, 37, and 47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the teachings of Voth in view of Kuribayashi.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for the respective details thereof.

## OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner and the evidence of anticipation and obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon does not support the Examiner's rejection of the claims on appeal. Accordingly, we reverse. In addition, we have *sua sponte* set forth new grounds of rejection for independent claim 1 pursuant to our authority under 37 C.F.R. § 41.50(b).

Independent claims 1, 38, 39 and 52

We consider first the Examiner's rejection of independent claims 1, 38, 39 and 52 as being anticipated by Voth.

Appellants argue that Voth fails to disclose, *inter alia*, "a processor interface *for interfacing the synchronization apparatus with a host processor"* (claim 1), "transmitting synchronization information and data to *a network in the control system*" (claims 1 and 38), "a second controller *outside the control chassis"* (claim 38), and a synchronization circuit that "is *configurable by the host processor* to operate as one of a synchronization master and a synchronization slave" (claims 39 and 52) (Br. 6-8, emphasis in original).

After carefully reviewing the multiple sections of the Voth reference relied upon by the Examiner, we conclude that the Examiner, as finder of fact, has not fully developed the record so as to clearly show how the elements of each independent claim are mapped to corresponding structures disclosed in the reference. In particular, we note the Examiner has merely provided *column and line number* citations in rejecting each independent claim. We find the Examiner's rejections fail to explain exactly how the Examiner is reading the language of each claim on the Voth reference. For us to affirm the Examiner on this record would require speculation on our part.

For example, Appellants argue the Examiner has mapped multiple features recited within the independent claims to single elements disclosed within the Voth reference. Appellants assert the Examiner has departed from the instant claimed structural relationships by corresponding Voth's "network 104" to both the claimed "processor interface" and the claimed

"network" (*See* Br. 6, ¶3). The Examiner merely responds that a processor interface for interfacing the synchronization apparatus with a host processor "exists between the time synchronization processor and the host" (Answer 21). However, we find the Examiner's response fails to directly address Appellants' argument that the Examiner has mapped multiple elements in the claim to a single element in the reference (e.g., "network 104"). Therefore, we agree with Appellants that the analysis set forth in the Answer fails to give proper consideration to distinct components having distinct structural relationships, as required by the language of each independent claim. To anticipate, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim. *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 927 F.2d 1565, 1576, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991). Thus, we conclude that the Examiner has failed to meet the burden of establishing a prima facie case of anticipation with respect to independent claims 1, 38, 39, and 52. Accordingly, we will reverse the Examiner's rejection of these claims as being anticipated by Voth.

Because we have reversed the Examiner's rejection of each independent claim, we will not sustain the Examiner's rejection of any of the dependent claims under appeal. Therefore, we reverse the Examiner's rejection of dependent claims 2-7, 13-28, 30-34, 40-46, and 48-51 as being anticipated by Voth. Likewise, we reverse the Examiner's rejection of dependent claims 8-12 as being unpatentable over Voth in view of

Rasmussen, and we also reverse the Examiner's rejection of dependent claims 29, 35-37, and 47 as being unpatentable over Voth in view of Kuribayashi.

## NEW GROUNDS OF REJECTION

Pursuant to our authority under 37 C.F.R. § 41.50(b), we have *sua sponte* set forth new grounds of rejection for independent claim 1.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by Esker (U.S. Patent 6,236,277).

| Instant claim 1 | Esker U.S. Pat. 6,236,277 |
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| 1. A time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising; | *See* the industrial controller time synchronization apparatus shown in Fig. 1 that consists of three controllers 12a-12c that form a control system where synchronization of the local clocks of controllers 12a-12c is performed by transmitting a "synchronizing message 52" from "master controller 12a" where "synchronizing message 52" consists of a timing pulse followed by a message indicating a master time value (col. 4, ll. 47-52, Fig. 1). |
| a processor interface for interfacing the synchronization apparatus with a host processor; | *See* "link circuit 27" (i.e., a processor interface) that provides the protocols necessary for communication between controllers (col. 4, ll. 28-32, Fig. 2). *See* "master controller 12a" (i.e., a host processor) (fig. 1, col. 4, ll. 47-49). Esker discloses that each controller |

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| | 12a-12c includes a "processor 20" (col. 4, ll. 12-13, Fig. 2). |
| a transmitter adapted to transmit synchronization information and data to a network in the control system; | *See* "I/O 30" that is a receiver/transmitter that transmits both synchronization information and data to "links 14" (i.e., a network") in the control system (col. 4, l. 20, Fig. 2). Esker discloses that "I/O 30" may be implemented in separate units (col. 4, ll. 6-7). *See* "synchronizing message 52" (i.e., synchronizing information) (col. 4, l. 50). Esker discloses that *both* synchronization information and data are transmitted, *see*, e.g., "The timing pulse may be very short and either an intrinsic part of the communication protocol or easily transmitted as a high priority message with little utilization of network bandwidth" (col. 4, ll. 53-56). |
| a receiver adapted to receive synchronization information and data from the network; and | *See* "I/O 30" that is a receiver/transmitter that transmits both synchronization information and data to "links 14" (i.e., a |

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| | network) in the control system (col. 4, ll. 2 and 20, Figs. 1-2). Esker discloses that *both* synchronization information and data are transmitted over the network (col. 4, ll. 53-56). |
| a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. | *See* "clock circuit 32" as shown in Fig. 2, and further shown in detail in Fig. 3. *See also* col. 4, ll. 36-46. Clock circuit 32 (i.e., in each non-master controller 12b-12c) is synchronized with a master time value generated remotely by one of the controllers (e.g., 12a) that serves as a master controller (i.e., host processor) whereby the master time value (i.e., indication of time) is received over "link 14" (i.e. a network) (col. 4, ll. 42-46). |

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by Yamanaka et al. (U.S. Patent 4,807,259).

| Instant claim 1 | Yamanaka U.S. Pat. 4,807,259 |
|---|---|
| 1. A time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising; | Yamanaka discloses an apparatus for synchronizing the time of a master clock at a master station (i.e., first controller) with slave clocks in slave stations (i.e., second controller). *See* Figs. 3A and 3B. Yamanaka discloses the stations (i.e., industrial controllers) are used to control and send commands to electrical power protection apparatus associated with electrical power transmission and power substation facilities (col. 1, ll. 15-22, col. 2, ll. 29-37). |
| a processor interface for interfacing the synchronization apparatus with a host processor; | Yamanaka discloses "master station 1" that includes "CPU 10" (i.e., a processor) that is operatively coupled to "code sending and receiving circuit 18" (i.e., a processor interface). *See* Fig. 3A and associated discussion col. 6, ll. 41-63. |

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| a transmitter adapted to transmit synchronization information and data to a network in the control system; | Yamanaka discloses "modem circuit 19" that transmits synchronization information and data to "external bus 5A" (i.e., a network) in the control system. *See* Fig. 3A and associated discussion col. 6, lines 41-63. Yamanaka explicitly discloses the transmission of *data and synchronization information* (col. 5, ll. 3-11). |
| a receiver adapted to receive synchronization information and data from the network; and | Yamanaka discloses a "slave station 2" that includes a "modem circuit 29" that receives synchronization information and data from "external bus 5A" (i.e., a network). See Fig. 3B and associated discussion col. 6, lines 41-63. *See also* col. 5, ll. 3-11, i.e., regarding the transmission of *data and synchronization information.* |
| a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. | Yamanaka discloses a "slave station 2" with a "slave clock 27" (i.e., a timing system) that maintains an indication of time according to information received from the host |

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| | processor (i.e., master station 1, CPU 10) via "external bus 5A" (i.e., a network). *See* Figs. 3A and 3B and associated discussion col. 4, ll. 6-14, and col. 6, ll. 41-63. |

## OTHER ISSUES

The Board of Patent Appeals and Interferences is a review body, rather than a place of initial examination. We have made a rejection above under 37 C.F.R. § 41.50(b). However, we have not reviewed claims 2-52 to the extent necessary to determine whether these claims are patentable over the Voth patent or other cited references. We leave it to the instant Examiner to determine the appropriateness of any further rejections based on these references.

## DECISION

In summary, we have reversed the Examiner's rejection of all the claims on appeal. Therefore, the decision of the Examiner rejecting claims 1-52 is reversed.

We have entered a new grounds of rejection against claim 1 under 37 C.F.R. § 41.50(b).

As indicated *supra*, this decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b) (amended effective September 13, 2004, by final rule notice 69 Fed. Reg. 49960 (August 12, 2004), 1286 Off. Gaz. Pat. & Trademark Office 21 (September 7, 2004)). 37 C.F.R. § 41.50(b) provides that "A new ground of rejection . . . shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner . . .
>
> (2) Request that the proceeding be reheard under § 41.52 by the Board upon the same record . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED.
37 C.F.R. § 41.50(b).

PGC

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